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# Experimental Analysis of Single Phase Bidirectional AC Buck Converter for Power Quality Improvement

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**ABSTRACT:** A novel bidirectional ac to ac buck converter circuit using power MOSFET operating in high frequency chopping mode is designed and analysed for parameters like input power factor, harmonic profile and efficiency of the converter. The equal PWM (EPWM) technique is a used to increase number of pulses per half cycle (P) in order to vary these parameters. The rms value of the fundamental component of the output voltage can be increased by varying the duty ratio (K) of the pulses. It is observed from the experimental results that the proposed scheme using EPWM technique significantly reduces low order harmonics, improves input power factor and efficiency and hence significantly reduces the filter size of the converter.

**Keywords:** AC chopper, AC snubbers, Harmonic Profile, equal PWM technique, Power quality.

## I. INTRODUCTION

Industrial loads such as heaters, illumination control, furnaces, AC motor speed control and also theatre dimmers uses AC voltage controllers. Such voltage regulators, however, have slow response, poor input power factor, and high magnitude of low order harmonic at both input and output sides. These converters need large input-output filters to reduce low order harmonics in the line current. These drawbacks have been overcome by designing various topologies of AC chopper [1-7]. In most standard AC choppers, the commutation causes high voltage spikes and an alternative current path has to be provided when current paths are changed. This alternative current path is implemented using additional bidirectional switches. Such topologies are difficult and expensive to realize and the voltage stress of the switch is also high, resulting in reduced reliability.

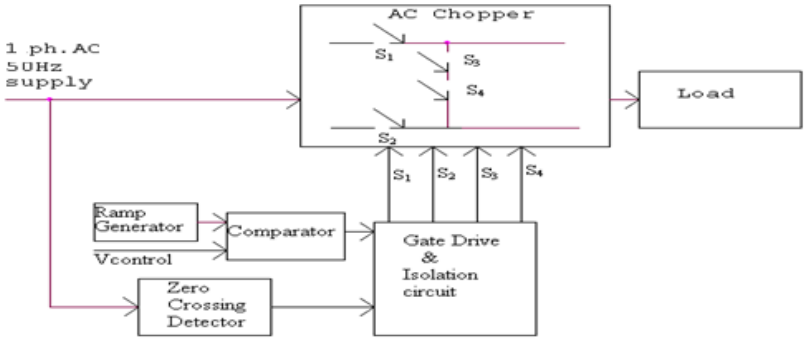


Fig. 1. Block Diagram of the proposed buck AC Chopper

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Fig.1 shows the block diagram of buck converter with control circuit to generate pulses to power MOSFET embedded four quadrant switches operating in high frequency chopping mode. In this paper, a novel bidirectional AC buck converter is proposed and analysed for RL load using EPWM technique where number of pulses per half cycle (P) is increased in order to change the harmonic profile of the output voltage and input source current. The power circuit is made up of a PWM buck chopper which uses four quadrant bidirectional switches. The AC voltage chopper is controlled using EPWM pattern which is efficient and simple to implement.

The control circuit comprises of 555 timer IC to generate saw tooth pulses of desired frequency which is compared with the variable DC voltage $V_{control}$ of amplitude 10 volts to generate switching pulses. The PWM pulses are given to the four switches through logic circuit, isolation circuit using opto-coupler MCT2E and gate drive circuit. The output voltage can be continuously varied by varying duty ratio (K) of the pulses. The technique continues to evoke interest with respect to variation of P and K [8]. The chopped output voltage waveform is analysed for harmonic content for various values of P & K. This technique can be adopted for the harmonic content reduction at the high frequency chopping mode facilitating easy filtration at lower cost.

## II. DESCRIPTION OF BUCK CONVERTER

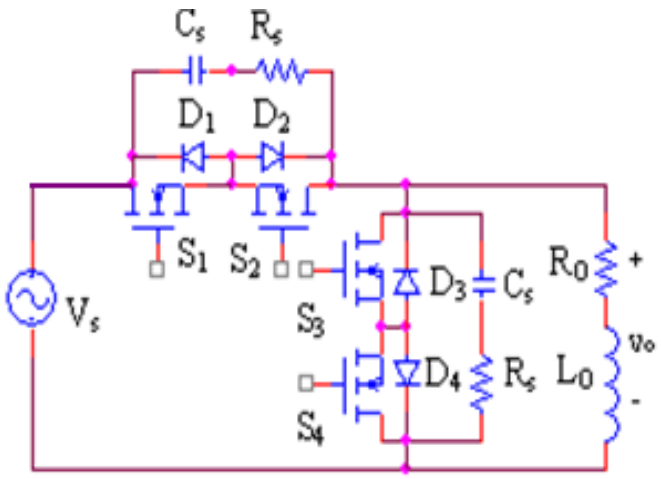


Fig.2. Single-phase Buck AC chopper using bidirectional switches and AC snubbers.

Fig. 2 shows Buck AC chopper derived from the DC buck chopper, where the normal unidirectional switches are replaced with four quadrant bidirectional switches. The combination of switches $S_1$ and $S_2$ along with body diodes forms one set of four quadrant switch for modulating purpose. Similarly the switch combination $S_3$ and $S_4$ form another four quadrant switch set for freewheeling operation with RL loads. The control of the switches is based on the EPWM technique. In practical realizations of the converter, stray inductances increase the voltage stress of the bidirectional switches and may destroy the switches. This situation requires the converter using AC snubber comprising RC combination ($R_s$ and $C_s$). In the configuration of the buck ac chopper, the commutation policy is that the switches $S_2$ and $S_4$ for $V_s > 0$ are additionally turned on during which switch $S_1$ is modulated. During negative half cycle, for $V_s < 0$, the switches $S_1$ and $S_3$ are turned on during which switch $S_2$ is modulated according to the duty ratio determined from the control strategy. If the load inductor current $i_L$ is positive, the inductor current is bypassed through output side using $S_4$ and diode $D_3$ across $S_3$. If the load inductor current is negative, the inductor current $i_L$ bypassed through the input side using $S_2$ and diode across $S_1$. The enhancement type MOFSETs are used in converters as switching devices due their high switching frequency greater than 1MHz, and is available with forward blocking voltage and current of 600V and 40A respectively. Operation of power switching devices at higher frequencies results in decreased size of inductors and filter capacitors that facilitates compact and economical power electronic systems.

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III. GENERATION OF GATE CONTROL SIGNALS

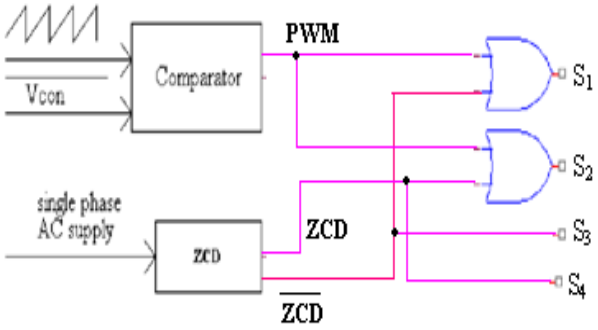


Fig. 3 Block diagram of the control circuit

Fig. 3 shows the block diagram of the control circuit. This circuit generates the PWM pattern gate control signals for four switches as that of the waveforms shown in the Fig. 5. The switching frequency is related to P and supply frequency f as

$$F_{sw} = 2Pf \qquad \text{---------- (1)}$$

The switching pulses obtained from control circuit is electrically isolated using opto-coupler IC MCT2E and given to the MOSFET switches IRFP460 through gate driver IC TC4424 for proper protection and switching operation. The phototransistor and driver IC is powered by an independent 5V source.

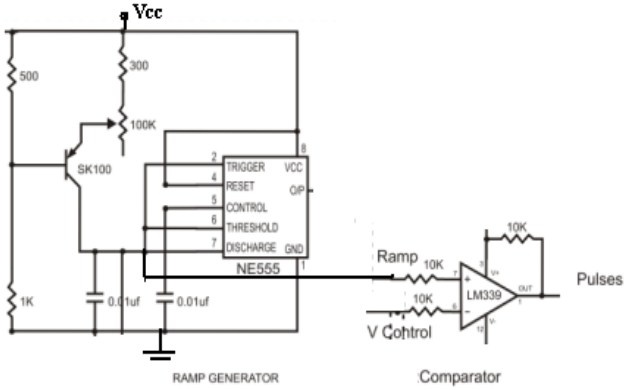


Fig. 4. EPWM pulses generated by comparing ramp with $V_{control}$

The EPWM pulses to be given to MOSFET switches are generated by comparing Ramp with control voltage $V_{control}$ as shown in Fig. 4. The capacitor is charged by a constant current source which causes the voltage across it to be linear ramp. The value of P can be selected by varying the variable potential divider connected to the emitter of the PNP transistor. The value of P is set for various carrier frequencies like 5 KHz, 7.5 KHz, 10 KHz, 15 KHz and 20 KHz to obtain the corresponding switching pulses. The value of the duty ratio K for every switching frequency can be varied by varying the control voltage $V_{control}$. The value of K is varied from 0.4 to 0.9 in order to vary the rms value of the fundamental component of the output voltage. The values of both P and K are varied in order to analyse the parameters like input power factor, Harmonic profile and efficiency of the converter.

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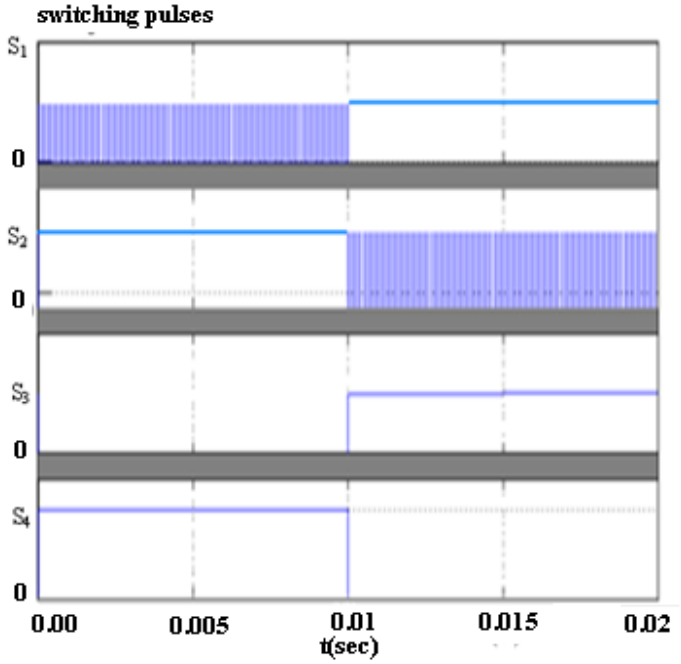


Fig.5. PWM pattern gate control signals.

## III. Experimental Results and Discussions

A Laboratory model of the single phase buck ac chopper as per the circuit shown in Fig. 2, is fabricated and tested for a load with parameters $R_L$=529Ω & $L_o$=100mH supplied with input voltage of 230V.

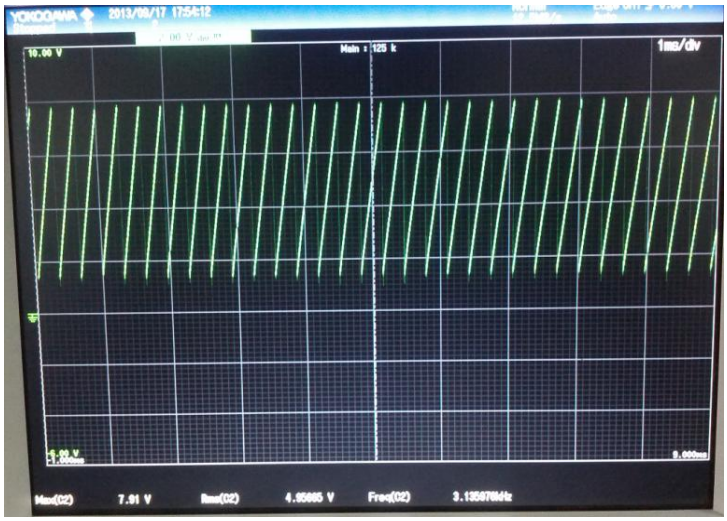

Fig. 6. Linear Ramp signal at the output of saw tooth generator

The carrier frequency ramp signal as shown in Fig. 6 is set for various switching frequencies of 5 KHz (P=50 as per equation (1)), 7.5 KHz (P=75), 10 KHz (P=100), 15 KHz (P=150) and 20 KHz (P=200). The control signals and output

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voltage waveforms are captured from two channelled 200MHz digital storage oscilloscope (DSO) model YOKOGAWA DLM2022, where the sampling rate is selected for 25K samples per window.

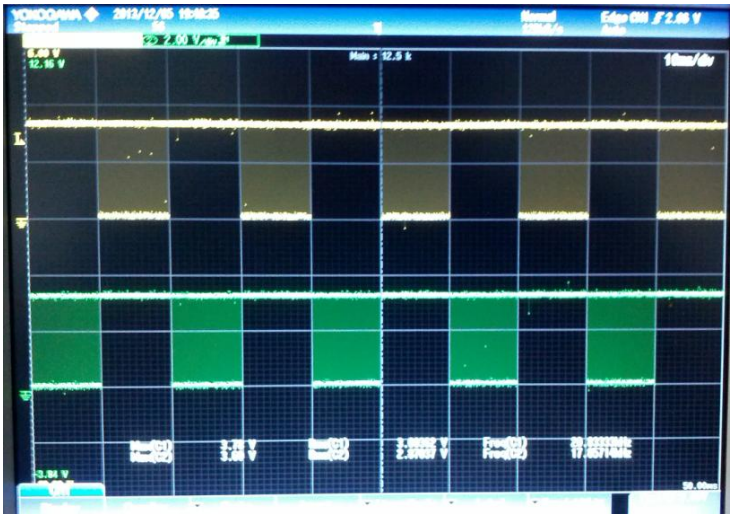

Fig. 7. Gate signal for MOSFETs $S_1$ and $S_2$ at P=200 & K=0.9

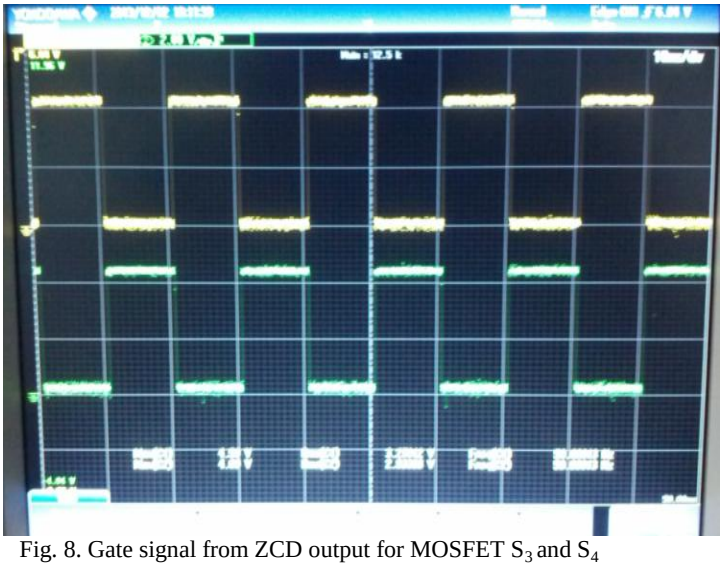

Fig. 8. Gate signal from ZCD output for MOSFET $S_3$ and $S_4$

Fig. 7 and 8 depicts the gate signals for the four MOSFETs of the converter as that of Fig. 5. The pulses obtained from comparator circuit is electrically isolated using opto coupler and given to switches through gate driver circuit.

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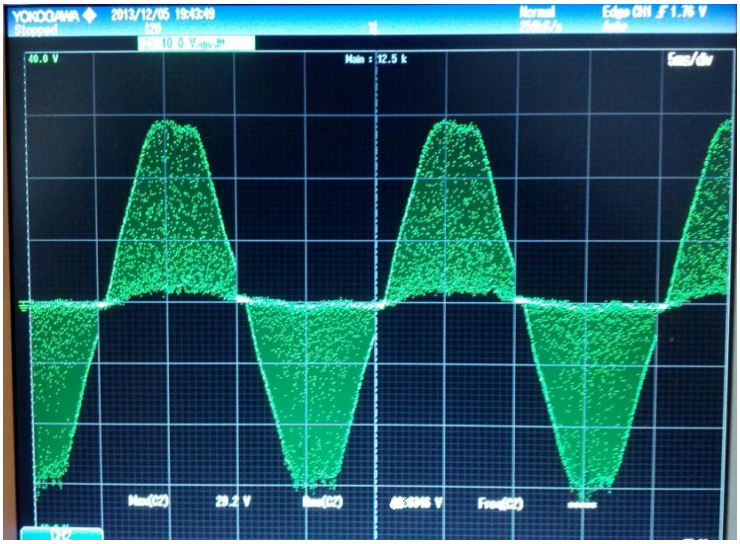

Fig. 9. Output voltage for P=200 and k=0.9

Fig. 9 depicts the output voltage waveform with respect to P=200 ($F_s$=20 KHz) and K=0.9 and the corresponding rms value is found to be 209V. The input power factor is increased from 0.7443 to 0.9789 by varying duty ratio from 0.4 to 0.9.

Table I
Variation of K and corresponding converter parameters

| P=200, Fs=20KHz | | | | | | |
|---|---|---|---|---|---|---|
| K | $V_{o\ in\ volt}$ | $I_{o\ in\ Amp}$ | $PF_{input}$ | THD(Vo) in %ge | THD(Is) in %ge | efficiency in %ge |
| 0.4 | 68 | 0.2257 | 0.7443 | 38.83 | 54.86 | 32.26 |
| 0.5 | 117 | 0.3037 | 0.85 | 28 | 42.8 | 52.56 |
| 0.6 | 154 | 0.36 | 0.903 | 11 | 29.57 | 67.99 |
| 0.7 | 174 | 0.3824 | 0.9386 | 10.78 | 26.84 | 75.51 |
| 0.8 | 206 | 0.42 | 0.9766 | 4.26 | 21.03 | 87.37 |
| 0.9 | 209 | 0.4223 | 0.9789 | 3.65 | 20.46 | 88.04 |

It is observed from Table I that THD of source current ($I_s$) and output voltage ($V_o$) are gradually reduced and efficiency of the converter is increased by increasing the value of K. The output voltage and current is increasing gradually with increase in K. The input power factor is 0.7443 at K=0.4 which is better than other switching frequencies. The THD of the output voltage and input source current is reduced drastically with the increase in the value of K. It is also observed that the losses in the converter are reduced with increase in power factor and hence correspondingly the efficiency of the converter is increased.

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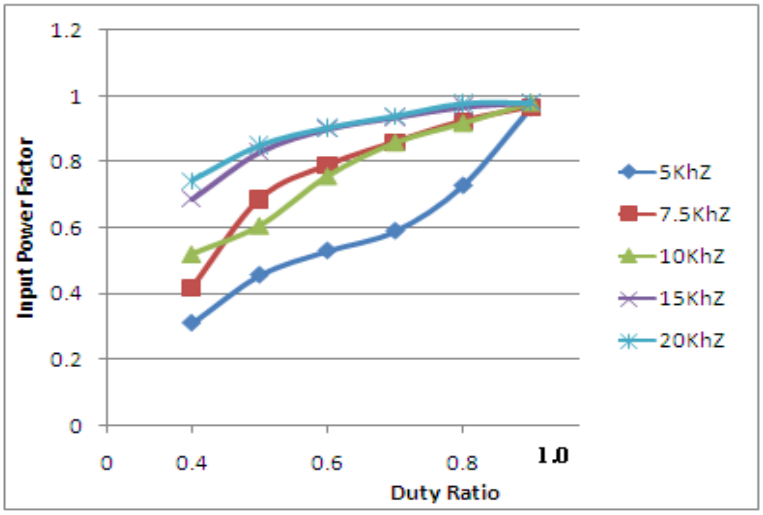


Fig. 10. Input power factor as a function of duty ratio K for different switching frequency.

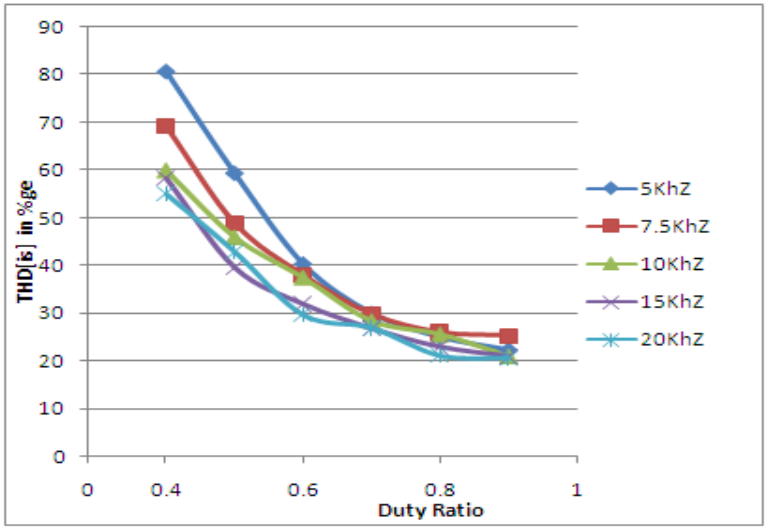


Fig. 11. THD (Is) as a function of duty ratio K for different switching frequency.

Fig. 10 and 11 depicts the input power factor and THD ($I_s$) as a function of duty ratio K varying from 0.4 to 0.9 for different values of switching frequencies from 5 KHz to 20 KHz. It is analysed from the plot that the input power factor is increased from 0.31 to 0.74 by increasing switching frequency from 5 KHz to 20 KHz with respect to duty ratio K=0.4 without using input filter elements. Therefore the EPWM technique increases the input power factor and reduces the corresponding total harmonic distortion of source current. The THD of the output voltage is reduced from 70.58% to 5.85% by varying K from 0.4 to 0.9 with respect to switching frequency of 5 KHz. In order to reduce the THD, the value of P is increased to 200, where the THD of the output voltage is reduced from 38.83% to 3.65% by varying K from 0.4 to 0.9 with respect to switching frequency of 20 KHz.

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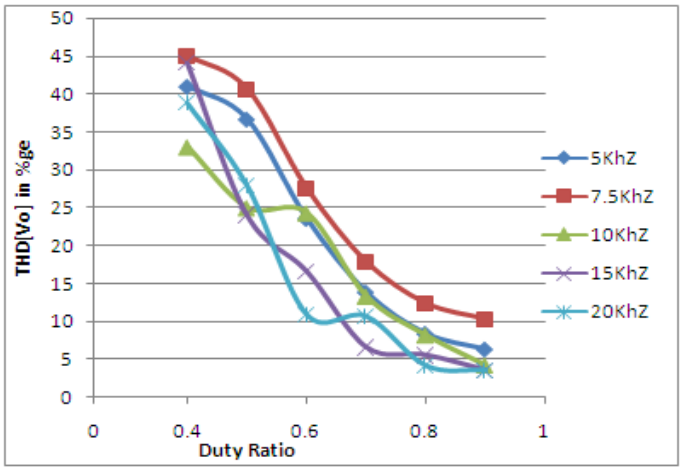


Fig. 12. THD ($V_o$) as a function of duty ratio K for different switching frequency.

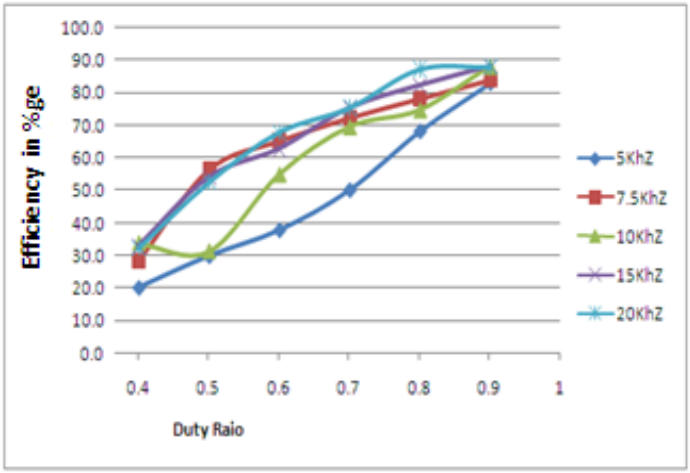


Fig. 13. Efficiency as a function of duty ratio K for different switching frequency.

The main advantage of choosing higher switching frequency is that the filter component size will be reduced that facilitates compact and economical power electronic system and also the fundamental component can be completely transferred to the output load. Fig. 12 depicts the THD of the output voltage as a function of duty ratio K for different switching frequencies. And Fig. 13 depicts the efficiency as a function of duty ratio K for different switching frequencies. It is observed from the above plots that by increasing the parameter P from 50 to 200, the input power factor and efficiency of the converter can be increased and THD of output voltage and source current can be reduced with the variation of K from 0.4 to 0.9. The experiment is conducted without any filter element at both input side and output side of the converter. It is observed that, the power quality can be improved with higher switching frequency with inclusion of small filter component both at input and output side of the converter circuit for best performance.

## IV. CONCLUSION

A single phase bidirectional AC Buck converter circuit using power MOSFET operating in high frequency chopping mode is designed implemented and analysed for parameters that includes input power factor, harmonic profile and efficiency of the converter fed to the RL load. The EPWM technique is a method where number of pulses per half cycle (P) is increased in order to improve these parameters. It is observed from the experimental results that the proposed scheme using EPWM technique significantly reduces low order harmonics, improves input power factor and efficiency

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of the converter and hence significantly reduces the filter size of the converter that facilitates compact and economical power electronic system.

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## BIOGRAPHY

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